CLAIMS

What is claimed is:

1. A light emitting diode comprising:

a first semiconductor layer doped with a first dopant, coupled to a first electrode layer;

an active layer overlying said first semiconductor layer, capable of emitting light;

a second semiconductor layer doped with a second dopant, overlying said active layer, said first dopant and said second dopant being of opposite type; and

a second electrode layer overlying said second semiconductor layer, wherein

at least one of said active layer and said second semiconductor layer has a periodically varying thickness with alternating maxima and minima, wherein

the ratio of the period of said periodic variation and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5; and

the thickness of said second semiconductor layer at said minima is less than about one wavelength of said emitted light in said second semiconductor layer.

2. The light emitting diode of claim 1, wherein

said first dopant is n-type and said second dopant is p-type.

3. The light emitting diode of claim 1, wherein

said first semiconductor layer overlies said first electrode layer.

4. The light emitting diode of claim 1, wherein

said first electrode layer partially overlies said first semiconductor layer; and

said first semiconductor layer overlies a substrate with a substantially reflective surface.

5. The light emitting diode of claim 1, wherein

said first electrode layer partially overlies said first semiconductor layer;

said second electrode layer is substantially reflective; and

said first semiconductor layer overlies a substantially transparent substrate.

6. The light emitting diode of claim 1, wherein

said first semiconductor layer, said active layer, and said second semiconductor layer have a surface recombination velocity less than 10^5 cm/sec.

7. The light emitting diode of claim 1, wherein

said first semiconductor layer, said active layer, and said second semiconductor layer comprise a group III element and a group V element.

8. The light emitting diode of claim 1, wherein

said first semiconductor layer, said active layer, and said second semiconductor layer comprise GaN.

9. The light emitting diode of claim 1, wherein

said periodically varying thickness is periodic in at least one direction parallel to the plane of said second semiconductor layer, wherein

said second semiconductor layer has a plane, and said plane has one or more directions.

10. The light emitting diode of claim 1, wherein

said second semiconductor layer has a planar lattice of through holes aligned with said minima.

11. The light emitting diode of claim 10, wherein

said active layer has a planar lattice of holes aligned with said planar lattice of through holes of said second semiconductor layer.

12. The light emitting diode of claim 11, wherein

said active layer has a planar lattice of through holes aligned with said planar lattice of through holes of said second semiconductor layer; and

said first semiconductor layer has a planar lattice of holes aligned with said planar lattice of through holes of said second semiconductor layer and said active layer.

13. The light emitting diode of claim 10, wherein

said planar lattice is a triangular lattice, square lattice, or a hexagonal lattice.

14. The light emitting diode of claim 10, wherein

said planar lattice is a honeycomb lattice.

15. The light emitting diode of claim 14, wherein

the intensity of said emitted light is substantially independent of the polarization, wherein said emitted light has an intensity and a polarization.

16. The light emitting diode of claim 10, wherein

said holes are filled with a dielectric.

17. The light emitting diode of claim 16, wherein

said dielectric is silicon oxide.

18. The light emitting diode of claim 1, wherein

the energy of said emitted light lies close to an edge of a band of the photonic band structure of said at least one of said active layer and said second semiconductor layer with periodically varying thickness, wherein

said at least one of said active layer and said second semiconductor layer has a photonic band structure, comprising one or more bands, having edges.

19. The light emitting diode of claim 18, wherein

the product of a rate of spontaneous emission and an efficiency of light extraction is greater at an energy close to said band edge than at a plurality of energies away from said band edge, wherein said light emitting diode has a rate of spontaneous emission and an efficiency of light extraction.

20. The light emitting diode of claim 16, wherein

the dielectric constants of said dielectric, said active layer and said second semiconductor layer assume values between about 1 and about 16; and

said holes occupy between about 10% and about 50% of the area of said second semiconductor layer.

21. The light emitting diode of claim 1, wherein

the intensity of light, emitted in the direction substantially normal to the plane of said second semiconductor layer, is greater, than the intensity of light, emitted in a direction substantially different from the normal of the plane of said second semiconductor layer, wherein said second semiconductor layer has a plane and a normal.

22. The light emitting diode of claim 1, wherein

said first semiconductor layer and said second semiconductor layer comprise AlInGaN;

said active layer comprises InGaN;

said first and second electrode layers comprise at least one of Ag, Al, and Au;

said periodic variation of thickness is a triangular lattice of holes, wherein

the diameter of said holes is between about 0.3a and about 0.72a, wherein

a is the period of the periodically varying thickness, and said holes have a diameter;

the depth of said holes is between about 0.375a and about 2a, wherein said holes have a depth;

said first and second semiconductor layers together form an epi-layer, having a thickness between about 0.375a and about 2a; and

said light, emitted by said active layer, has a frequency between about 0.66(c/a) and about 0.75(c/a), wherein c is the speed of light in air.

23. The light emitting diode of claim 1, wherein

said first semiconductor layer and said second semiconductor layer comprise AlInGaN;

said active layer comprises InGaN;

said first and second electrode layers comprise at least one of Ag, Al, and Au;

said periodic variation of thickness is a triangular lattice of holes, wherein

the diameter of said holes is between about 0.3a and about 0.72a, wherein

a is the period of the periodically varying thickness, and said holes have a diameter;

the depth of said holes is greater than about 2a, wherein said holes have a depth;

said first and second semiconductor layers together have a thickness greater than about 4a; and

said light, emitted by said active layer has a frequency in one of the ranges of about 0.275(c/a) to about 0.375(c/a) and about 0.58(c/a) to about 0.68(c/a), wherein c is the speed of light in air.

24. The light emitting diode of claim 1, wherein

said light emitting diode is disposed in a package, the package comprising:

a support frame;

a heat sink disposed within said support frame for extracting heat from said light emitting diode, wherein

said light emitting diode is disposed over said heat sink;

a plurality of leads, electrically coupled to said light emitting diode; and

a transparent housing.

25. A light emitting diode comprising:

a first semiconductor layer doped with a first dopant;

an active layer overlying said first semiconductor layer, capable of emitting light; and

a second semiconductor layer doped with a second dopant overlying said active layer, said first and second dopants being of opposite type, wherein

at least one of said active layer and said second semiconductor layer has a periodically varying thickness with alternating maxima and minima, wherein

the ratio of the period of said periodic variation and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5; and

the thickness of said second semiconductor layer at said minima is less than about one wavelength of said emitted light in said second semiconductor layer; and

at least one of said first semiconductor layer, said active layer, and said second semiconductor layer comprises a group III element and a group V element.

26. The light emitting diode of claim 25, wherein said group III element is Gallium, and the group V element is Nitrogen.

27. The light emitting diode of claim 25, wherein

said first semiconductor layer and said second semiconductor layer have a surface recombination velocity less than 10^5 cm/sec.

28. The light emitting diode of claim 25, wherein

said first dopant is n-type and said second dopant is p-type.

29. The light emitting diode of claim 25, wherein

said first semiconductor layer overlies said first electrode layer.

30. The light emitting diode of claim 25, wherein

said first electrode layer partially overlies said first semiconductor layer; and

said first semiconductor layer overlies a substrate with a substantially reflective surface.

31. The light emitting diode of claim 25, wherein

said first electrode layer partially overlies said first semiconductor layer;

said second electrode layer is substantially reflective; and

said first semiconductor layer overlies a substantially transparent substrate.

32. The light emitting diode of claim 25, wherein

said periodically varying thickness is periodic in at least one direction parallel to the plane of said second semiconductor layer, wherein

said second semiconductor layer has a plane, and said plane has one or more directions.

33. The light emitting diode of claim 25, wherein

said second semiconductor layer has a planar lattice of through holes aligned with said minima.

34. The light emitting diode of claim 33, wherein

said active layer has a planar lattice of holes aligned with said planar lattice of through holes of said second semiconductor layer.

35. The light emitting diode of claim 34, wherein

said active layer has a planar lattice of through holes aligned with said planar lattice of through holes of said second semiconductor layer; and

said first semiconductor layer has a planar lattice of holes aligned with said planar lattice of through holes of said second semiconductor layer and said active layer.

36. The light emitting diode of claim 33, wherein

said planar lattice is a triangular lattice, a square lattice, or a hexagonal lattice.

37. The light emitting diode of claim 33, wherein

said planar lattice is a honeycomb lattice.

38. The light emitting diode of claim 37, wherein

the intensity of said emitted light is substantially independent of the polarization, wherein said emitted light has an intensity and a polarization.

39. The light emitting diode of claim 33, wherein

said holes are filled with a dielectric.

40. The light emitting diode of claim 39, wherein

said dielectric is silicon oxide.

41. The light emitting diode of claim 25, wherein

the energy of said emitted light lies close to an edge of a band of the photonic band structure of said at least one of said active layer and said second semiconductor layer with periodically varying thickness, wherein

said at least one of said active layer and said second semiconductor layer with periodically varying thickness has a photonic band structure, comprising one or more bands, having edges.

42. The light emitting diode of claim 41, wherein

the product of a rate of spontaneous emission and an efficiency of light extraction is greater at an energy close to said band edge than at a plurality of energies away from said band edge, wherein said light emitting diode has a rate of spontaneous emission and an efficiency of light extraction.

43. The light emitting diode of claim 39, wherein

the dielectric constants of said dielectric, said first semiconductor layer, and said second semiconductor layer assume values between about 1 and about 16; and

said holes occupy between about 10% and about 50% of the area of said second semiconductor layer.

44. The light emitting diode claim of 25, wherein

the intensity of light, emitted in the direction substantially normal to the plane of said second semiconductor layer, is greater, than the intensity of light, emitted in a direction substantially different from the normal of the plane of said second semiconductor layer, wherein said second semiconductor layer has a plane and a normal.

45. The light emitting diode of claim 25, wherein

said first semiconductor layer and said second semiconductor layer comprise AlInGaN;

said active layer comprises InGaN;

said periodically varying thickness is a triangular lattice of holes, wherein

the diameter of said holes is between about 0.3a and about 0.72a, wherein

a is the period of the periodically varying thickness, and said holes have a diameter;

the depth of said holes is between about 0.375a and about 2a, wherein said holes have a depth;

said first and second semiconductor layers together form an epi-layer, having a thickness between about 0.375a and about 2a; and

said light, emitted by said active layer, has a frequency between about 0.66(c/a) and about 0.75(c/a), wherein c is the speed of light in air.

46. The light emitting diode of claim 25, wherein

said first semiconductor layer and said second semiconductor layer comprise AlInGaN;

said active layer comprises InGaN;

said periodically varying thickness is a triangular lattice of holes, wherein

the diameter of said holes is between about 0.3a and about 0.72a, wherein

a is the period of the periodically varying thickness, and said holes have a diameter;

the depth of said holes is greater than about 2a, wherein said holes have a depth;

said first and second semiconductor layers together have a thickness greater than about 4a; and

said light, emitted by said active layer has a frequency in one of the ranges of about 0.275(c/a) to about 0.375(c/a) and about 0.58(c/a) to about 0.68(c/a), wherein c is the speed of light in air.

47. A method of making a light emitting diode, the method comprising:

providing a semiconductor structure, comprising:

a substrate;

a plurality of semiconductor layers, capable of emitting light, overlying said substrate;

a top electrode layer, overlying said plurality of semiconductor layers; and

a photosensitive layer overlying said top electrode layer, having a planar lattice of openings, wherein

the ratio of the period of said planar lattice of openings and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5; and

forming a planar lattice of holes by removing said top electrode layer and at least partially removing said plurality of semiconductor layers at regions corresponding to said planar lattice of openings.

48. The method of claim 47, wherein the providing the semiconductor structure comprises:

forming a first semiconductor layer doped with a first dopant, overlying said substrate;

forming an active layer, capable of emitting said light, overlying said first semiconductor layer;

forming a second semiconductor layer doped with a second dopant, said first and second dopant being of opposite type, overlying said active layer.

49. The method of claim 48, wherein said forming of said planar lattice of holes comprises:

forming said planar lattice of holes in at least said active layer and in said second semiconductor layer.

50. The method of claim 48, wherein said providing of semiconductor structure comprises:

removing said second semiconductor layer and said active layer over a region of said first semiconductor layer, displaced from said planar lattice of holes;

forming a first electrode layer overlying of a portion of said displaced region of said first semiconductor layer.

51. The method of claim 47, wherein said providing of semiconductor structure comprises:

forming said substrate with a substantially reflective surface.

52. The method of claim 47, wherein said providing of semiconductor structure comprises:

forming said substrate from a substantially transparent material; and

forming said top electrode layer from a substantially reflective material.

53. The method of claim 47, wherein said providing of semiconductor structure comprises:

forming a first electrode layer on the side of the substrate opposite to said plurality of semiconductor layers.

54. The method of claim 47, wherein said providing of said photosensitive layer having a planar lattice of openings comprises:

removing portions of said photosensitive layer in a planar lattice of openings with a high resolution lithographic technique.

55. The method of claim 54, wherein said removing of said photosensitive layer with a high resolution lithographic technique comprises:

removing of said portions of said photosensitive layer with electron beam lithography, nano-imprint lithography, deep X-ray lithography, interferometric lithography, hot embossing, or microcontact printing.

56. The method of claim 47, wherein said forming of holes comprises:

forming of said planar lattice of holes by a dry process.

57. A method of making a light emitting diode, the method comprising:

providing a semiconductor structure, comprising:

a first substrate;

a masking layer with a first planar lattice of openings, overlying said substrate;

a plurality of semiconductor layers, capable of emitting light, overlying said first substrate, wherein

the ratio of the period of said planar lattice of openings and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5; and

forming a planar lattice of holes in said plurality of semiconductor layers by at least partially removing said plurality of semiconductor layers in regions corresponding to said first planar lattice of openings of said masking layer.

58. The method of claim 57, wherein said providing said semiconductor structure comprises:

forming a first semiconductor layer doped with a first dopant, overlying said masking layer and said first substrate;

forming an active layer, overlying said first semiconductor layer, wherein said active layer is capable of emitting said light; and

forming a second semiconductor layer doped with a second dopant, said first and second dopant being of opposite type, overlying said active layer.

59. The method of claim 58, wherein said forming of said first semiconductor layer, said active layer, and said second semiconductor layer comprises:

forming said first semiconductor layer, said active layer, and said second semiconductor layer with an epitaxial lateral overgrowth technique.

60. The method of claim 59, further comprising:

forming a bonding layer overlying said second semiconductor layer;

forming a second substrate overlying said bonding layer; and

removing said first substrate.

61. The method of claim 60, further comprising:

removing said masking layer;

forming a first electrode layer overlying said first semiconductor layer by depositing said first electrode layer at an angle to have no substantial electrical contact between said first electrode layer and said second semiconductor layer; and

forming a second electrode layer overlying a region of said second semiconductor layer displaced from said planar lattice of holes.

62. The method of claim 60, wherein said forming of said planar lattice of holes comprises:

forming a photosensitive layer overlying said masking layer;

exposing said photosensitive layer at regions corresponding to said first lattice of openings of said masking layer by shining a light from the direction of said second substrate.

63. The method of claim 62, wherein said forming of said planar lattice of holes comprises:

forming a lattice of aligned mask-layers corresponding to said first planar lattice of openings of said first masking layer by

removing a portion of said photosensitive layer, overlying said first masking layer, leaving said exposed regions of said photosensitive layer; and

removing said first masking layer from said first semiconductor layer.

64. The method of claim 63, further comprising:

forming a first electrode layer, overlying said first semiconductor layer and said aligned mask-layers.

65. The method of claim 64, further comprising:

forming a second planar lattice of openings in said first electrode layer by removing said lattice of aligned mask-layers and portions of said first electrode layer overlying said aligned mask-layers with a lift-off technique.

66. The method of claim 65, further comprising:

forming a planar lattice of holes by at least partially removing said plurality of semiconductor layers in regions corresponding to said second planar lattice of openings in said first electrode layer.

67. The method of claim 66, further comprising:

forming a second electrode layer overlying a region of said second semiconductor layer displaced from said lattice of holes.

68. The method of claim 67, wherein

said forming of said first electrode layer and said second electrode layer comprises:

forming at least one of said first electrode layer and said second electrode layer from a substantially reflective material; and

said forming of said second substrate comprises:

forming said second substrate from a substantially transparent material.

69. The method of claim 67, wherein

said forming of said second substrate comprises:

forming said second substrate with a substantially reflective surface.

70. The method of claim 57, further comprising:

removing said first masking layer to expose a surface of said first semiconductor layer.

71. The method of claim 70, further comprising:

filling up said lattice of holes with a dielectric to form an approximately flat surface with said exposed surface of said first semiconductor layer; and

forming a first electrode layer overlying said approximately flat surface.

72. The method of claim 71, further comprising:

forming a second electrode layer overlying a region of said second semiconductor layer displaced from said lattice of holes.

73. The method of claim 72, wherein

said forming of said first electrode layer and said second electrode layer comprises:

forming at least one of said first electrode layer and said second electrode layer from a substantially reflective material; and

said forming of said second substrate comprises:

forming said second substrate from a substantially transparent material.

74. The method of claim 72, wherein

said forming of said second substrate comprises:

forming said second substrate with a substantially reflective surface.

75. A method of making a light emitting diode, the method comprising:

providing a semiconductor structure, comprising:

a substrate;

a masking layer with a first planar lattice of openings, overlying said substrate;

a plurality of semiconductor layers, overlying said masking layer; and

a photosensitive layer, overlying said plurality of semiconductor layers;

shining light at said first planar lattice of openings from the direction of said substrate; and

creating images of said openings of said first planar lattice of openings on said photosensitive layer by causing the diffraction of said shined light.

76. The method of claim 75, wherein the providing of a semiconductor structure comprises:

forming said substrate;

forming said masking layer with a first planar lattice of openings, overlying said substrate;

forming a first semiconductor layer doped with a first dopant, overlying said masking layer;

forming an active layer, overlying said first semiconductor layer, wherein said active layer is capable of emitting light; and

forming a second semiconductor layer doped with a second dopant, overlying said active layer, said first and second dopant being of opposite type, wherein

the ratio of the period of said planar lattice of openings and the wavelength of said emitted light in air is greater than about 0.1 and less than about 5.

77. The method of claim 76, wherein said forming of said first semiconductor layer, said active layer, and said second semiconductor layer comprises:

forming said first semiconductor layer, said active layer, and said second semiconductor layer with an epitaxial lateral overgrowth technique.

78. The method of claim 76, wherein said providing a plurality of semiconductor layers comprises:

forming said plurality of semiconductor layers with a total thickness proportional to the square of the lattice spacing of said first planar lattice of openings, and proportional to the inverse of the wavelength of said emitted light in said plurality of semiconductor layers, wherein

said first planar lattice of openings has a lattice spacing and said emitted light has a wavelength in said plurality of semiconductor layers.

79. The method of claim 75, wherein said creating of images comprises:

creating images of said openings of said first planar lattice of openings by shining said light from a near-collimated light source.

80. The method of claim 76, further comprising:

forming a second planar lattice of openings in said photosensitive layer by removing said photosensitive layer at regions corresponding to said images of said openings of said first planar lattice of openings.

81. The method of claim 80, further comprising:

forming a planar lattice of holes in said plurality of semiconductor layers by at least partially removing said plurality of semiconductor layers in regions corresponding to said second planar lattice of openings; and

removing said photosensitive layer, exposing a surface of said second semiconductor layer.

82. The method of claim 81, further comprising:

forming a first electrode layer overlying a region of said first semiconductor layer displaced from said planar lattice of holes; and

forming a second electrode layer overlying said second semiconductor layer by depositing said second electrode layer at an angle to have no substantial electrical contact between said second electrode layer and said first semiconductor layer.

83. The method of claim 81, further comprising:

filling up said planar lattice of holes with a dielectric to form an approximately flat surface with said exposed surface of said second semiconductor layer; and

forming a second electrode layer overlying said approximately flat surface.

84. The method of claim 83, further comprising:

forming a first electrode layer overlying a region of said first semiconductor layer displaced from said planar lattice of holes.

85. The method of claim 84, wherein

said forming of said first electrode layer and said second electrode layer comprises:

forming at least one of said first electrode layer and said second electrode layer from a substantially reflective material; and

said forming of said substrate comprises:

forming said substrate from a substantially transparent material.

86. The method of claim 84, wherein

said forming of said substrate comprises:

forming said substrate with a substantially reflective surface.

87. The method of claim 75, further comprising:

forming a lattice of aligned mask-layers from said photosensitive layer by removing said photosensitive layer except at regions corresponding to said images of openings of said first planar lattice of openings.

88. The method of claim 87, further comprising:

forming a second electrode layer overlying said plurality of semiconductor layers and said lattice of aligned mask-layers; and

forming a second planar lattice of openings in said second electrode layer by removing said lattice of aligned mask-layers and the corresponding overlying portions of said second electrode layer.

89. The method of claim 88, further comprising:

forming a planar lattice of holes in said plurality of semiconductor layers by at least partially removing said plurality of semiconductor layers at regions corresponding to said second planar lattice of openings.

90. The method of claim 89, further comprising:

forming a first electrode layer overlying a region of said first semiconductor layer displaced from said planar lattice of holes.

91. The method of claim 90, wherein

said forming of said first electrode layer and said second electrode layer comprises:

forming at least one of said first electrode layer and said second electrode layer from a substantially reflective material; and

said forming of said substrate comprises:

forming said substrate from a substantially transparent material.

92. The method of claim 90, wherein

said forming of said substrate comprises:

forming said substrate with a substantially reflective surface.